ABSTRACT

A pipelined processor such as an averaging filter including at least one subtractor section and at least one adder section. Both of the subtractor section and the adder section have a plurality of adder logic units. In comparison to the conventional processor, the processor of the present invention is streamlined by the application of one or more of three techniques. First, there is the interleaving approach where the subtractor section and the adder section are interleaved with one another. Second, there is the one delay feedback approach where the adder section includes a one delay feedback for each of the adder logic units. Third, there is the delay enable signal output approach where the averaging filter includes a delay enable signal output for each of the adder logic units of the adder section.